

Fig. 1

NVIC Control Table

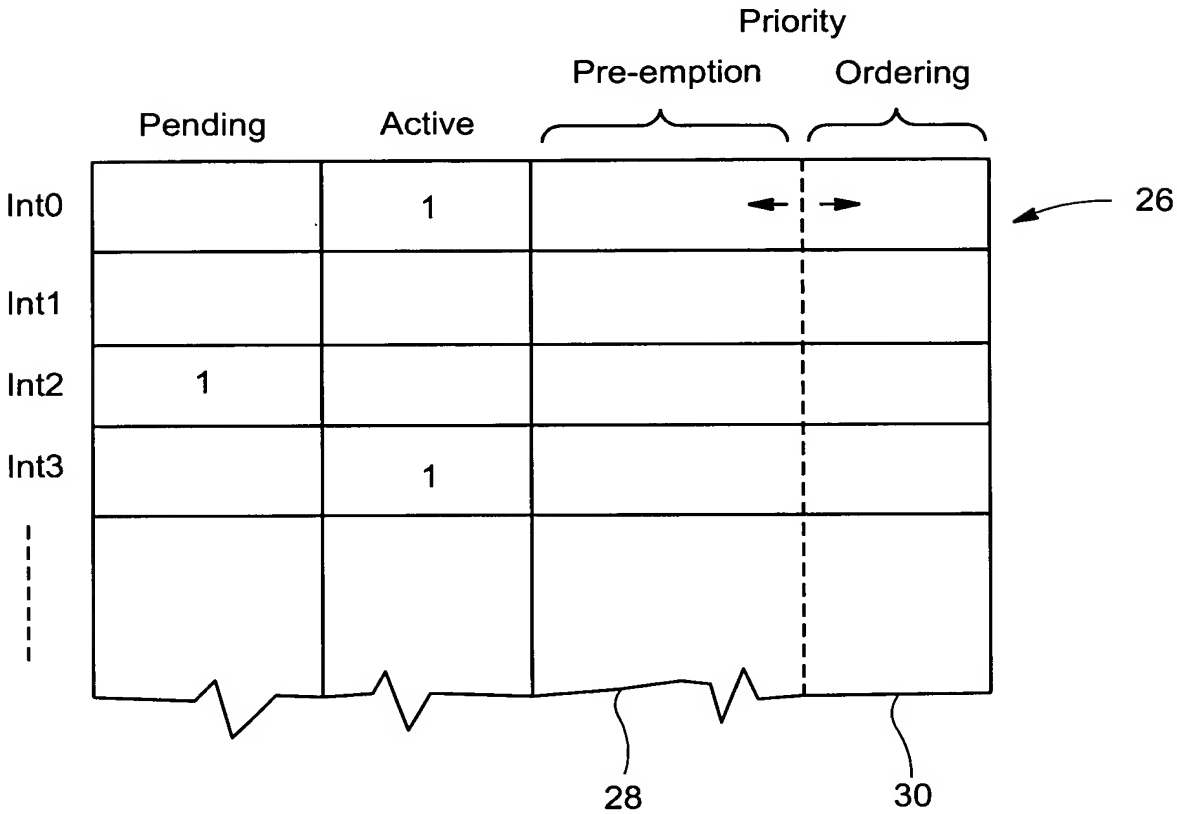


Fig. 2

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## Stack Memory

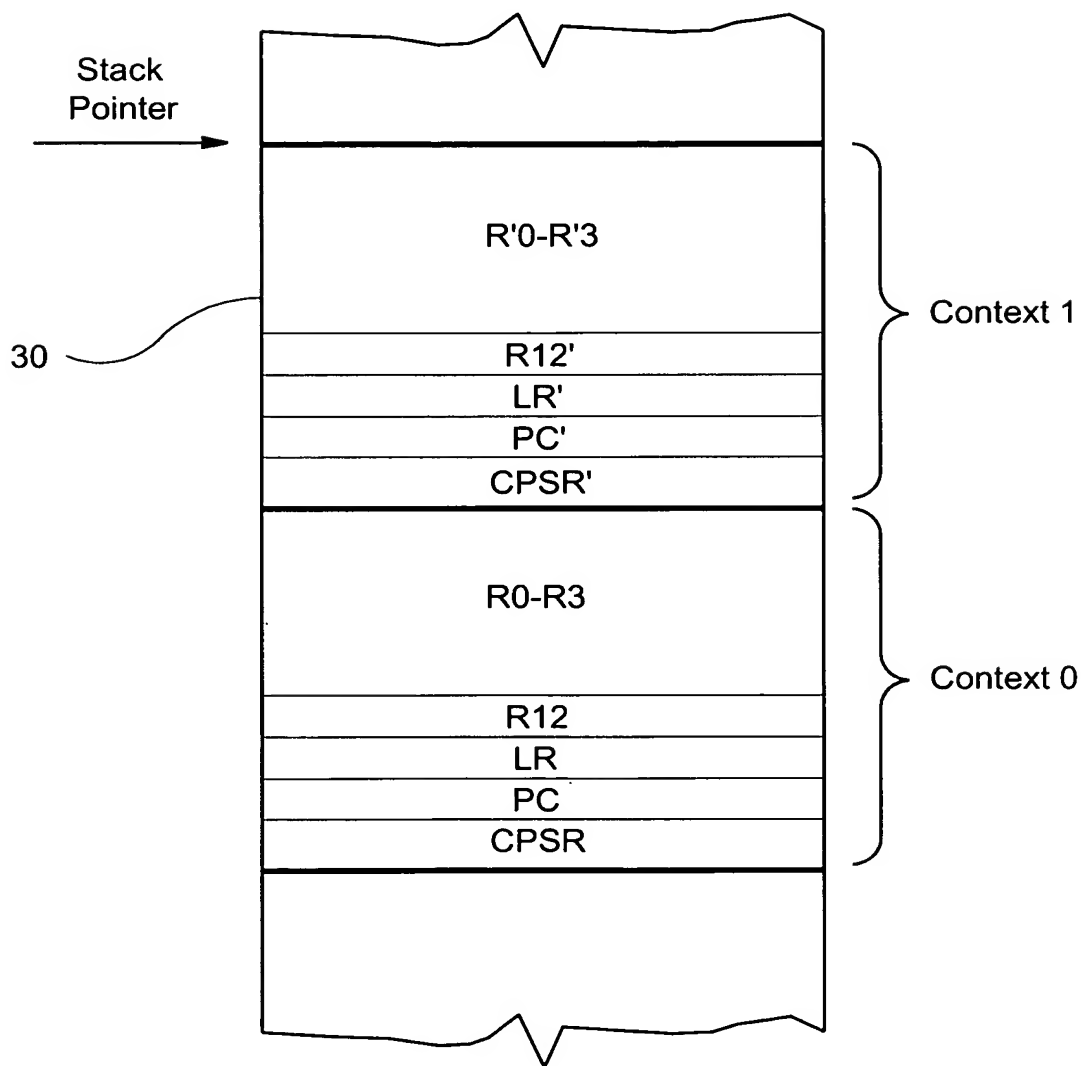


Fig. 3

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## Priority Inversions

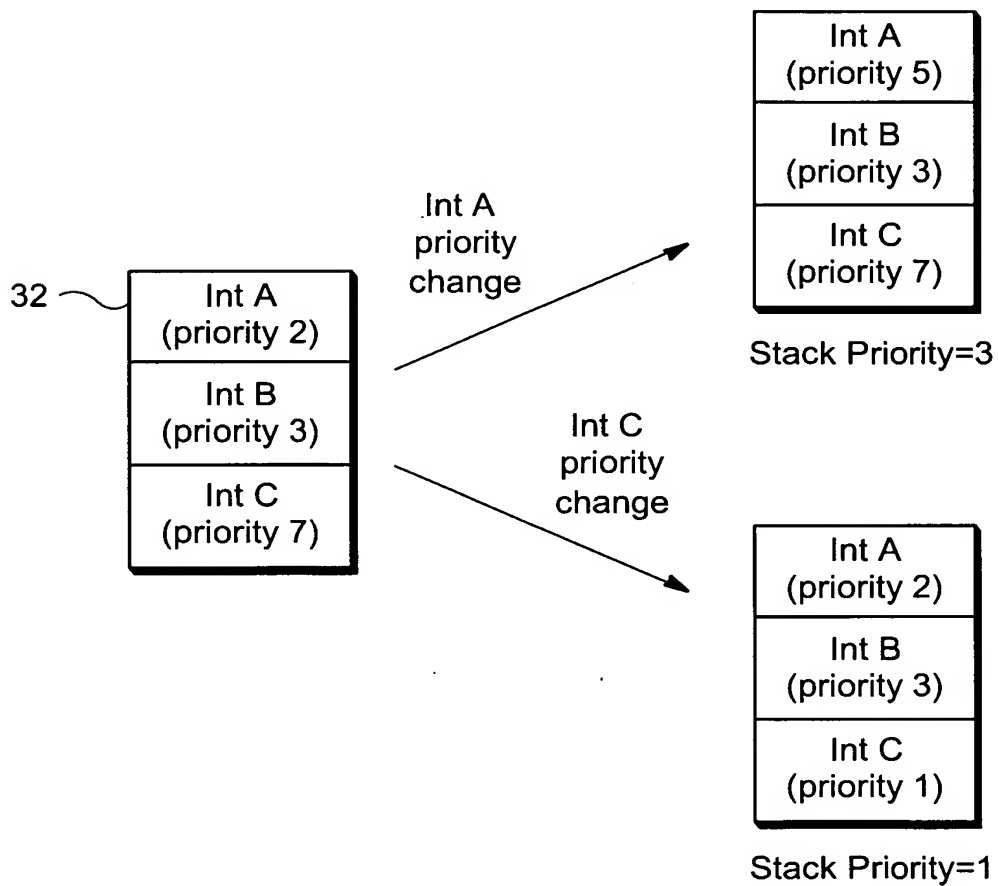


Fig. 4

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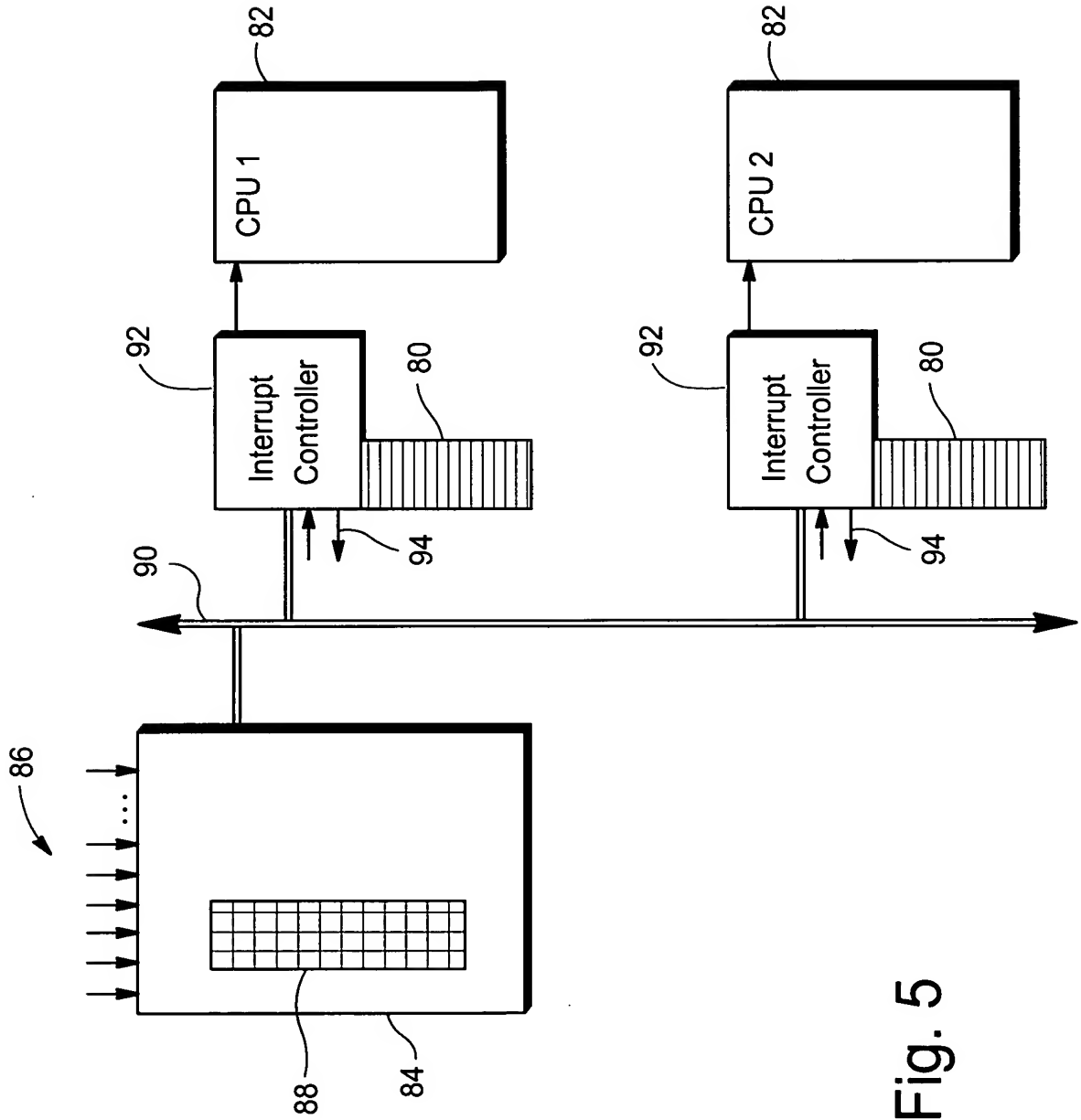


Fig. 5

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## Main Flow

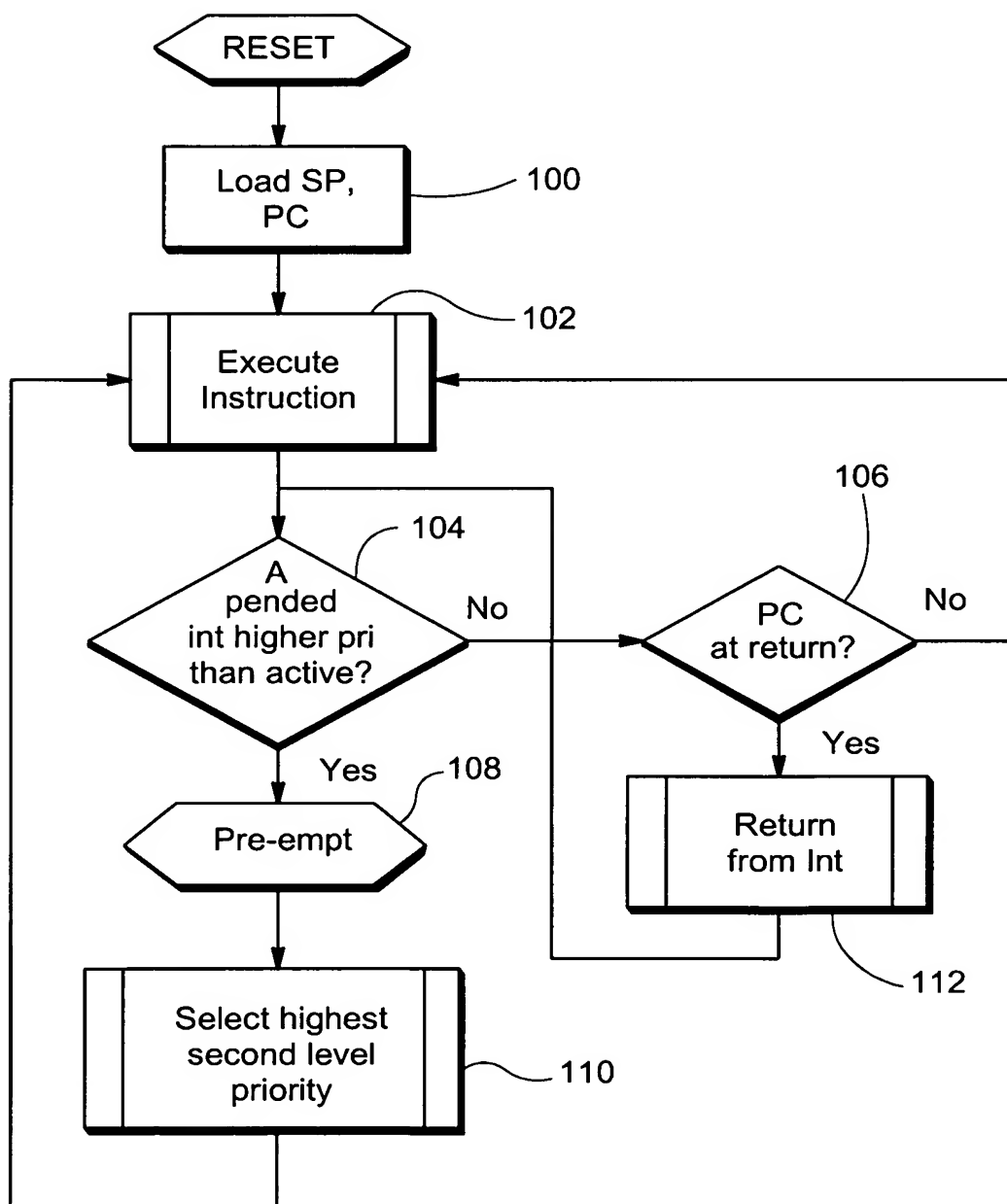


Fig. 6

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## Main Flow with Tail Chaining

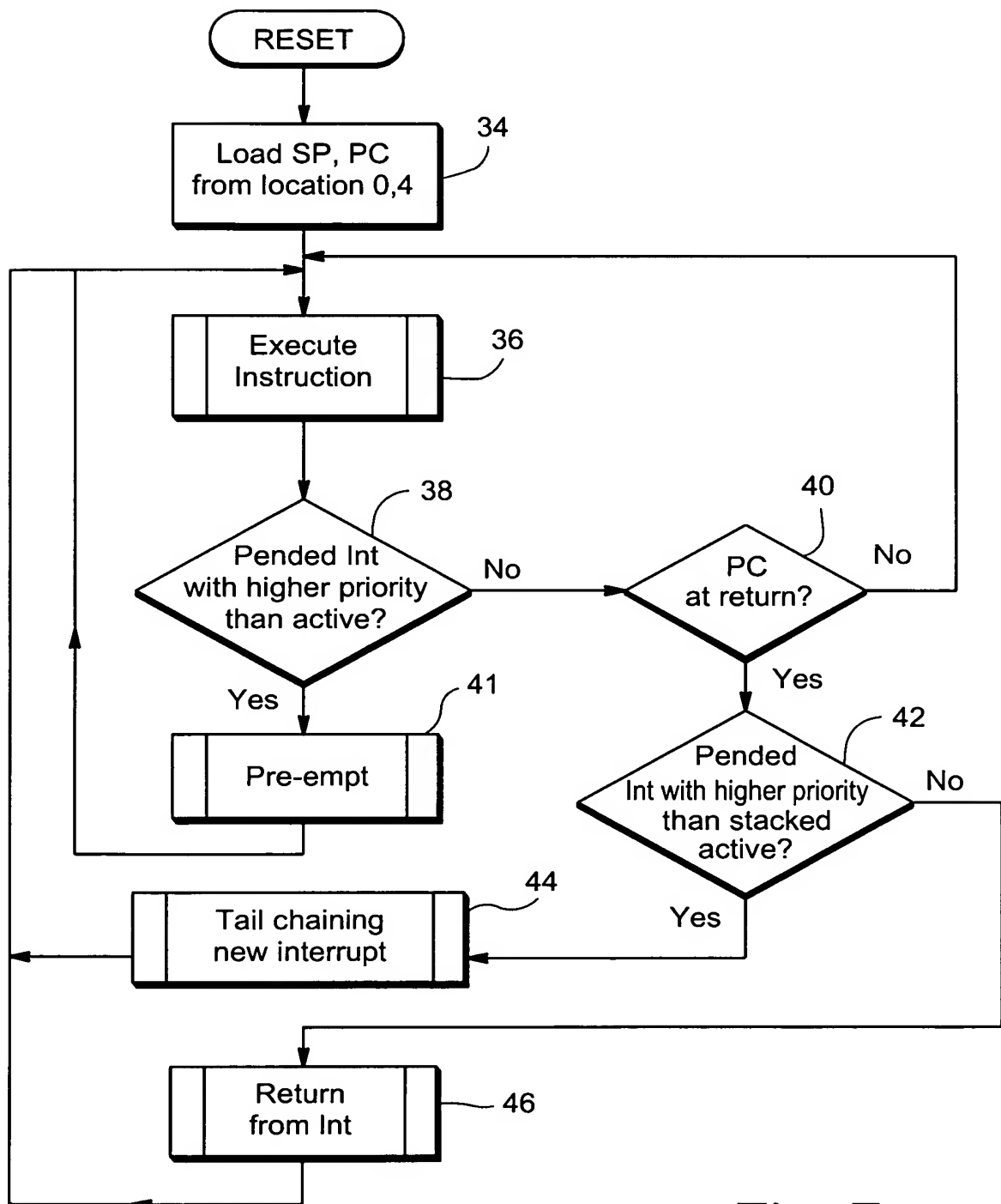


Fig. 7

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## Pre-emption Flow

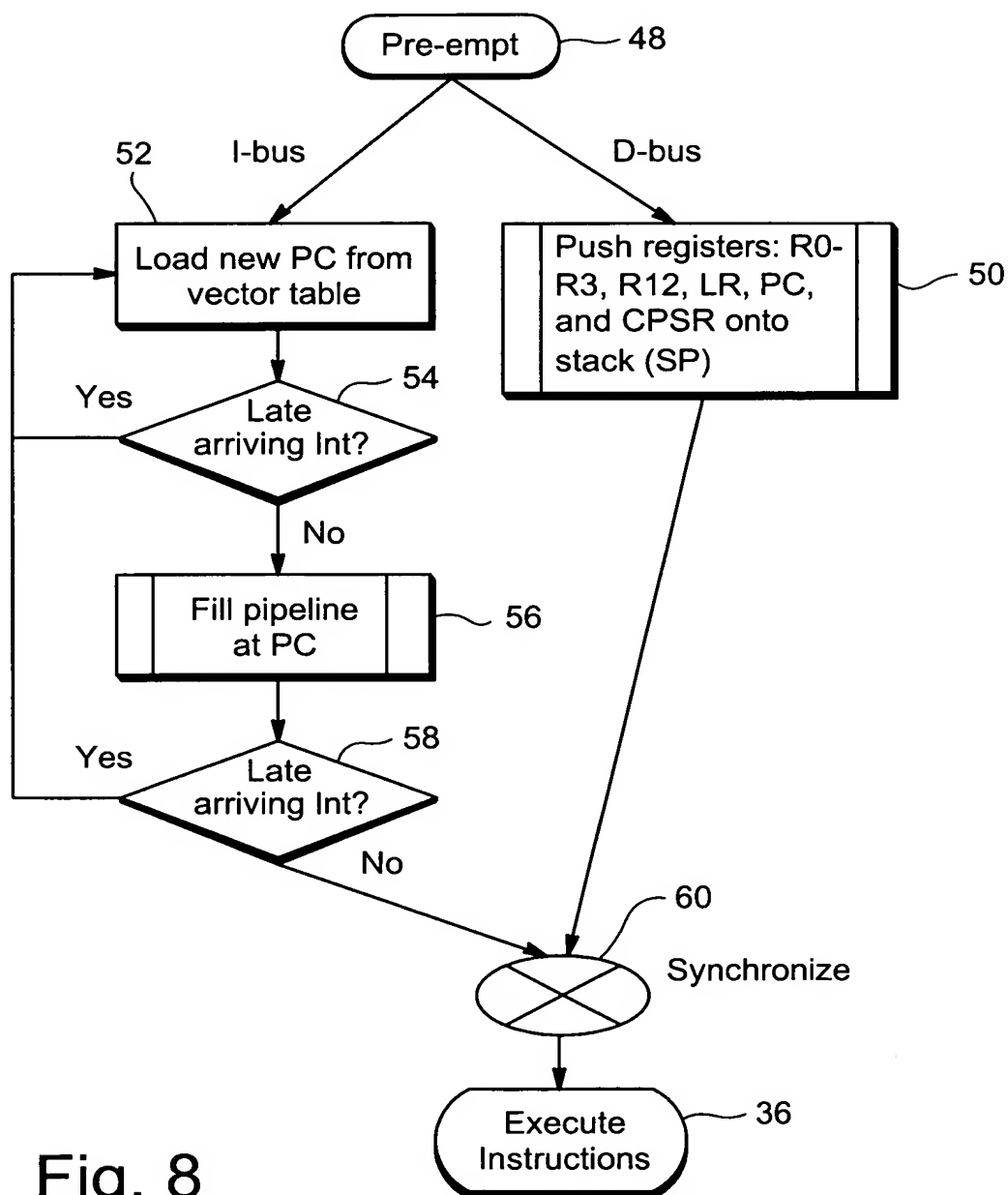


Fig. 8



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## Return From Interrupt Flow

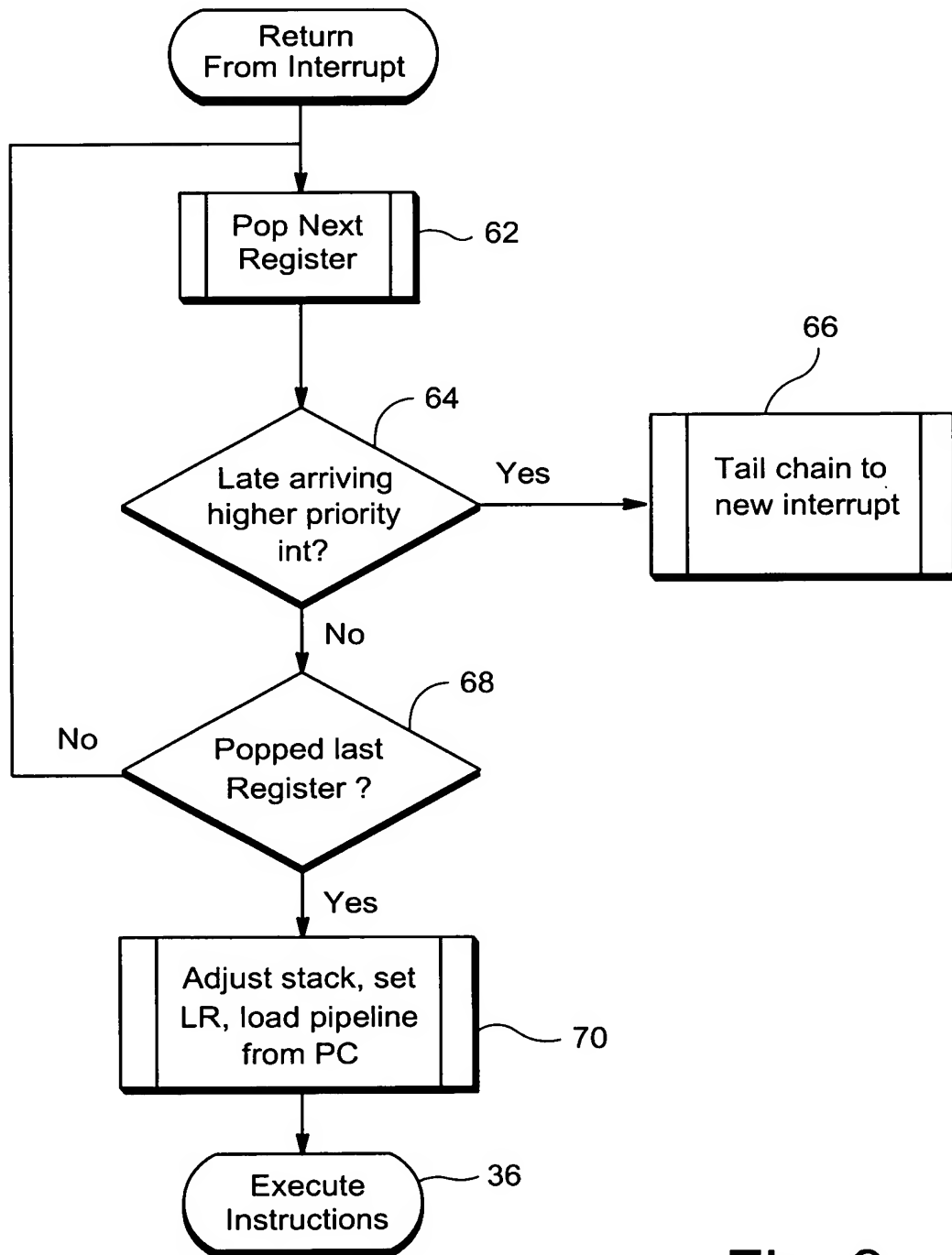


Fig. 9

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## Tail Chaining Flow

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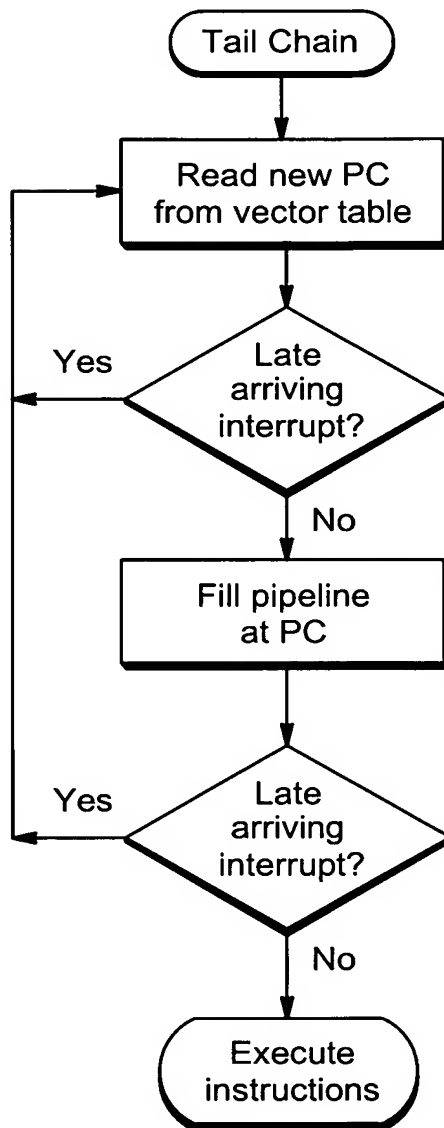


Fig. 10